IN THE SPECIFICATION:

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] As BGA packages migrate toward higher connection ~~densities~~ densities, such as Fine Pitch Ball Grid Arrays (FBGA) and Extra Fine ~~pitch~~ Pitch Ball Grid Arrays ~~(EFBGA)~~ (EFBGA), some additional problems become more severe. The trend toward higher speeds in smaller packages creates both thermal and electrical problems. As semiconductor package size decreases, operating frequencies increase, circuit densities increase, and significant heat is generated, which must be dissipated away from the die as effectively as possible. Heat dissipation is a particular problem with a smaller package where there is less surface area for heat dissipation. These problems of providing structural stiffness and heat dissipation have been addressed in the past. Kinsman et al. in Patent 6,268,650 and Castro et al. in Patent 6,300,165 each address semiconductor device assemblies providing enhanced thermal performance with added structural stiffness.

Please replace paragraph number **[0008]** with the following rewritten paragraph:

[0008] One exemplary embodiment of the invention comprises a semiconductor device assembly comprising a semiconductor die attached to an electrically conductive layer with a dielectric adhesive, which may be thermally conductive. The semiconductor die has bond pads in a row, or a plurality of parallel rows, extending substantially along the center of the die. The electrically conductive layer contains a longitudinal slot configured ~~such,~~ such that when the semiconductor die is attached to the electrically conductive layer, the bond pads are exposed through the slot. The electrically conductive layer provides thermal conduction to draw heat away from the semiconductor die and structural stiffness to the final semiconductor device assembly. In addition, the electrically conductive layer provides a voltage reference plane that may be connected to a power source, a ground source, or an intermediate reference voltage source. The electrically conductive layer also includes at least one additional slot referred to as an electrical current isolation slot. The electrical current isolation slot, or slots, segments the

electrically conductive layer to help isolate noise induced in one segment of the electrically conductive layer from the other segments.

Please replace paragraph number **[0012]** with the following rewritten paragraph:

[0012] This embodiment is configured to receive the semiconductor die, which may be attached to the electrically conductive layer with a thermally ~~conductive,~~ conductive dielectric adhesive. Additionally, this embodiment is configured to receive solder balls in a grid array on top of the dielectric film and bonding wires to connect the conductive traces and the electrically conductive layer to the semiconductor die.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] Another exemplary embodiment of the invention comprises a semiconductor device assembly comprising a semiconductor die attached to an electrically conductive layer with a dielectric adhesive, which may be thermally conductive. In this exemplary embodiment, the bond pads may be located around the periphery of the semiconductor die. The electrically conductive layer covers a portion of the semiconductor die such that the bond pads around the periphery are exposed. Additionally, the electrically conductive layer contains at least one current isolation slot. However, the conductive layer need not contain a longitudinal slot. A dielectric film is attached to the electrically conductive layer comprising a pattern of conductive traces extending between bonding landing areas near the periphery of the dielectric film and ball placement locations distributed across the dielectric film. Additionally, the dielectric film includes one or more conductive vias formed therethrough connecting one or more conductive traces on the top surface of the dielectric film to the electrically conductive layer adhered to the bottom surface of the dielectric film. Bonding wires connect the electrically conductive layer to one or more bond pads on the semiconductor die, which are configured for connection to the desired voltage reference. Additional bonding ~~wired~~ wires connect other bond pads on the semiconductor die to conductive traces on the electrical connection layer. Discrete conductive ~~elements~~ elements, such as solder ~~balls~~ balls, disposed on the dielectric film provide structural

and electrical connection for the semiconductor die through their associated conductive traces to an external system ~~substrate~~ substrate, such as a circuit board.

Please replace paragraph number **[0016]** with the following rewritten paragraph:

[0016] FIG. 1 is ~~eross~~ cross-sectional view of an exemplary semiconductor device assembly of the present invention;

Please replace paragraph number **[0019]** with the following rewritten paragraph:

[0019] FIG. 4 is a ~~eross~~ cross-sectional view of a multi-layer substrate including a plurality of conductive layers according to the present invention;

Please replace paragraph number **[0020]** with the following rewritten paragraph:

[0020] FIG. 5 is a ~~eross~~ cross-sectional view of another exemplary embodiment of the semiconductor device assembly of the present invention with bond pads around the periphery of a semiconductor die; and

Please replace paragraph number **[0023]** with the following rewritten paragraph:

[0023] High frequency signals, particularly those with fast edge rates may induce considerable noise in power and ground planes. This noise may be introduced from many sources. Two of the most serious sources are capacitive coupling and ground bounce. Capacitive coupling may occur between two separate but adjacent conductors carrying electrical signals. A coupling effect is created through an electrical field existing in a dielectric material separating these conductors. The dielectric material may simply be air or may be any other ~~non~~ nonconductive material separating the adjacent signal conductors. Capacitive coupling between a reference power source and a transitioning signal generally helps reduce noise and ringing on the transitioning signal. However, at the same time, it can introduce noise into the reference power source. A large plane of low impedance material connected to the reference power source reduces this noise or at least localizes the noise to a very small area near the conductor containing the transitioning signal.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] FIG. 2 depicts current isolation slots 124 extending from proximate the longitudinal slot 126 to proximate the laterally peripheral edges of the electrically conductive layer 120. FIGS. 3A and 3B show other examples of how the current isolation slots 124 may be located and configured on the electrically conductive layer 120. In FIG. ~~3A~~ 3A, the current isolation slots 124 extend ~~from~~ from, and are contiguous ~~with~~ with, the longitudinal slot 126 to proximate the laterally peripheral edges of the electrically conductive layer 120. In FIG. ~~3B~~ 3B, the current isolation slots 124 extend ~~from~~ from, and ~~intersect~~ intersect, the laterally peripheral edges of the electrically conductive layer 120 to proximate the longitudinal slot 126.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] ~~FIG. 5~~FIG. 5 depicts another exemplary embodiment of the semiconductor device assembly 100 comprising a semiconductor die 110 with the bond pads 112 disposed around the periphery of the semiconductor die 110 rather than along the center of the semiconductor die 110. In this embodiment, the electrically conductive layer 120 covers only the portion of the die between the bond pads 112 on the periphery of the semiconductor die 110 such that the bond pads 112 are exposed. As shown in FIG. 6A, electrical current isolation slots 124 suitable for use in this embodiment may extend from proximate one peripheral edge to proximate the laterally opposite peripheral edge of electrically conductive layer 120. Additionally, electrical current isolation slots 124 may be ~~non-~~nonlinear. Electrical current isolation slots 124 may, for example, form an L shape or a U-~~shape~~ shape, as shown in FIG. 6C. As another example, electrical current isolation slots 124 may form diagonal lines relative to the peripheral edges of the electrically conductive layer ~~120~~ 120, as shown in FIG. 6B.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] FIGS. 1, 2, and 5 also show a dielectric film 130, which may comprise a polyimide film such as ~~KAPTON®~~ KAPTON® polymer. As can be seen in FIGS. 1 and 5, the dielectric film 130 is attached to the surface of the electrically conductive layer 120 on the side opposite the semiconductor die 110. The dielectric film 130 provides an electrically insulative

layer on the electrically conductive layer 120. In FIG. 2, the dielectric film 130 includes a longitudinal slot 136 therethrough similar in placement to the longitudinal slot 126 in the electrically conductive layer 120. However, the longitudinal slot 136 is wider than the longitudinal slot 126 such that an electrical conductor landing area 128 is exposed on the electrically conductive layer 120. This electrical conductor landing area 128 provides a place for bonding wires to bond to the electrically conductive layer 120 on one side and bond pads 112 on the semiconductor die 110 on the other side. For a semiconductor die 110 with bond pads 112 around the periphery of the semiconductor die, as shown in FIG. 5, the dielectric film 130 may be somewhat smaller than the electrically conductive layer 120 such that an electrical conductor landing area 128 is exposed around the periphery of the electrically conductive layer 120 where bonding to the electrically conductive layer is desired.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] As shown in FIG. 4, the dielectric film 130 may also be fabricated as a ~~multi-~~multilayer dielectric film 139 comprised of additional electrical connection layers, each including conductive traces 132′ and additional dielectric layers 130′ disposed therebetween. Multiple layers of conductive traces 132′ may aid in signal routing for complex designs. In some complex ~~designs~~ designs, placement of discrete conductive elements 150, such as solder balls, may not match with bond pads 112 on the semiconductor die 110 in such a way as to facilitate direct routing on a single layer from the bond wire landings 133 to the locations of ~~solder balls~~ discrete conductive elements 150. Interlayer conductive vias 138 enable connection between conductive traces 132′ of different additional electrical connection layers as well as connection to conductive traces 132 on the top electrical connection layer. The conductive vias 134 for connecting between the electrically conductive layer 120 and the ~~top electrical connection layer~~ conductive traces 132 are formed through all dielectric layers (*i.e.*, film 130 and layer 130′) and in isolation from conductive traces (132 and 132′). By way of example, FIG. 4 shows conductive traces 132’ for two additional electrical connection layers and two additional interposed dielectric layers 130′. However, many numbers and configurations of the ~~electrical connection layers~~

conductive traces 132 and dielectric ~~layers~~ film 130 are possible within the scope of the present invention.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] The discrete conductive elements 150 such as solder ~~balls 150~~ balls, may be formed or disposed on the conductive traces 132 of ~~the~~ an electrical connection layer ~~132~~. These ~~solder balls~~ discrete conductive elements 150 create the means for physically attaching and electrically coupling the semiconductor device assembly 100 to an external system substrate (not shown). These discrete conductive elements 150 are typically formed of solder but may be in the form of other package connection ~~means~~ means, such as stud bumps, plated bumps, conductive polymers, or conductor-filled polymers.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] A dielectric encapsulant 160 well known in the art, such as an epoxy resin, may be used to provide protection from damage and the elements by covering the bond pads 112 of the semiconductor die 110 exposed through the longitudinal slot 126 and ~~bond~~ bonding wires 142, as shown in broken lines in FIG. 1. Dielectric encapsulant 160 may, for example, comprise a silicone-filled thermoplastic resin applied by transfer molding or injection molding. Dielectric encapsulant 160 may also be applied using stereolithographic techniques, with a photocurable polymer.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] A method of producing the semiconductor device assembly 100 is described. The electrical current isolation slots 124 and longitudinal slot 126 (if present) may be formed in the electrically conductive layer 120 by means well known in the ~~art~~ art, such ~~as~~ as by stamping, chemical etching, electro-discharge machining (EDM), or laser ablation. As noted above, a desirable number, location, and configuration of the electrical current isolation slots 124 may be determined based on the architecture and characteristics of the semiconductor die 110 to be attached or the system substrate to which the semiconductor device 100 will be attached.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] The dielectric film 130 is adhered to one side of the electrically conductive layer 120. Adhesion may be accomplished with many techniques well known in the art, such ~~as,~~ as by using ~~use of~~ a thermoset or thermoplastic adhesive. As part of the fabrication process, conductive vias 134 may be formed through the dielectric film 130 and filled with a conductive material to connect to the electrically conductive layer 120 such that the conductive vias 134 can conduct heat and electrical current to and from the electrically conductive layer 120. Conductive vias 134 may be filled using stencils, screen-printing, electroplating, or ~~electro~~ electroless plating, as known in the art.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] Discrete conductive elements 150 are ~~formed~~ formed, or ~~disposed~~ disposed, in array ~~fashion~~ fashion, on the top of the dielectric film 130 such that they connect to the conductive vias 134 and conductive traces 132 of the electrical connection layer formed on the dielectric film 130 after dielectric encapsulant 160 is applied. A semiconductor die 110 is attached to the bottom surface of the electrically conductive layer 120 using a thermally conductive dielectric adhesive layer 118 well known in the art, such ~~as,~~ as thermoset adhesives, thermoplastic adhesives, and adhesive tape. Bond pads 112 are electrically connected to the conductive traces 132 of the electrical connection layer on the dielectric film 130 using a conventional wire bonding technique. Similarly, bond pads 112 connected to the desired voltage source are electrically connected to the electrically conductive layer ~~120.~~ 120 using a conventional wire bonding technique. After wire bonding, the bond pads 112 of the semiconductor die 110 exposed through the longitudinal slot 126 and ~~bond~~ bonding wires 142 may be covered with a dielectric encapsulant 160, as known in the art, for protection from physical damage and the environment.